PVP 14

Code: EE5T6

III B.Tech - I Semester – Regular/Supplementary Examinations
March - 2021

LINEAR AND DIGITAL INTEGRATED CIRCUIT APPLICATIONS

(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1.

a) Brief the importance of CMRR and Slew rate of op-amp.
b) Draw the circuit to generate sine wave for input cosine wave using op-amp.
c) Discuss the Barkhausen criterion for oscillations with example.
d) Write the formula of output of inverting summer using op-amp.
e) Describe the working of Voltage controlled oscillator in communications systems.
f) Define the capture and lock range of PLL.
g) Illustrate the design procedure of combinational circuits.
h) Perform the conversions i) $(12345)_8=(\ )_{12}$,
ii) $(5459)_{10}=(\ )_7$
i) Compare and contrast latch and Flip-flop.
j) Design mod 4 counter.
k) Design 4bit adder unit.

PART – B

Answer any *THREE* questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Derive the inverting and non inverting gains of an op-amp and describe its block diagram. 8 M

b) Design a circuit using op-amp to generate an output $Vo = sin(2at)$ for the input signal cos (at). 8 M

3. a) Design a Square and Triangular wave generator for input sine wave. 8 M

b) Design a wide band-pass filter with fH=200Hz, fL=1KHz and a pass-band gain=4. Draw the frequency response and calculate Q factor for the filter. 8 M

4. a) Draw the circuit diagram of IC555 astable multivibrator and explain. 8 M

b) Illustrate the block schematic of PLL in detail. 8 M

5. a) Implement the 16 input to 4 output priority encoder. 8 M

b) Design a 4×4 combinational multiplier. 8 M

6. a) Draw the logic diagram of universal shift register and explain its operation. 8 M

b) Design a 4bit up counter. 8 M